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Publication Classification

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(57) **ABSTRACT**

An active matrix organic electroluminescent display device of the present invention is fabricated through a six-mask process unlike the related art that uses eight masks. In the present invention, since the ground line and the power line are entirely disposed above the substrate, the resistance of the power line is reduced and the thermal damage that may occur in the power line during driving the device is prevented. Therefore, the image quality increases and the uniformity in the display can be obtained. Furthermore, due to the reduction of the mask process, the occurrence of defects is reduced and the production yield can be raised. Additionally, the principles of the present invention can be applied to either the top emission type organic electroluminescent display device or the bottom emission type organic electroluminescent display device. When it is utilized for the top emission type, the active matrix organic electroluminescent display device can have a high aperture ratio.

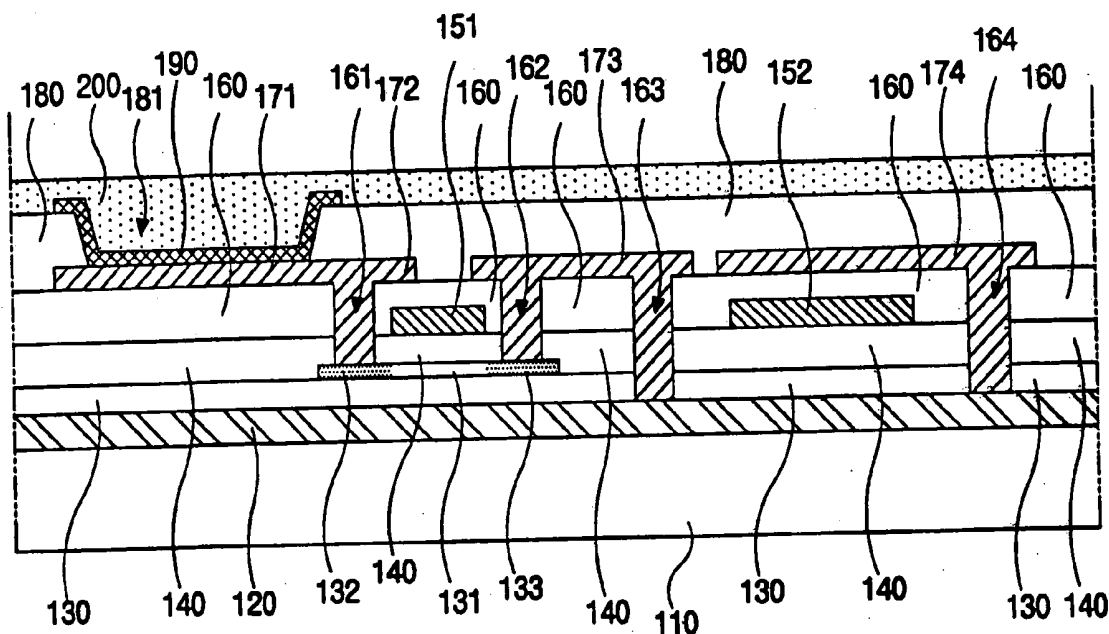
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(30) **Foreign Application Priority Data**

Dec. 29, 2001 (KR) 2001-88538



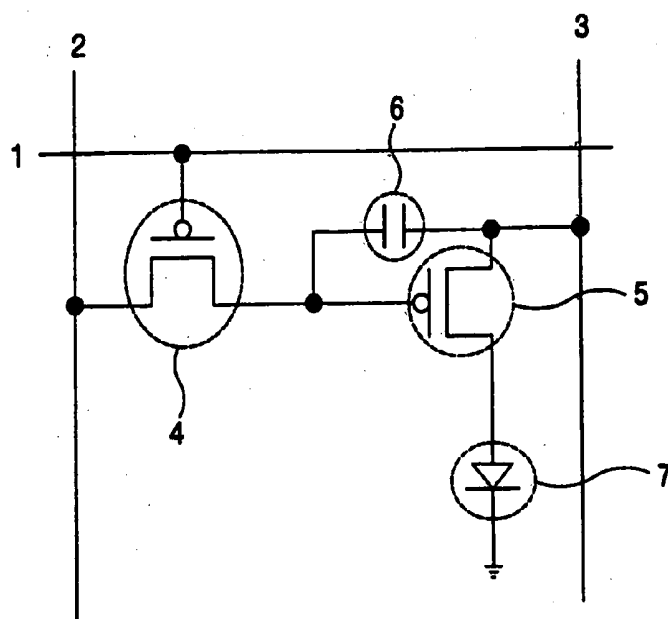


FIG. 1
(Related Art)

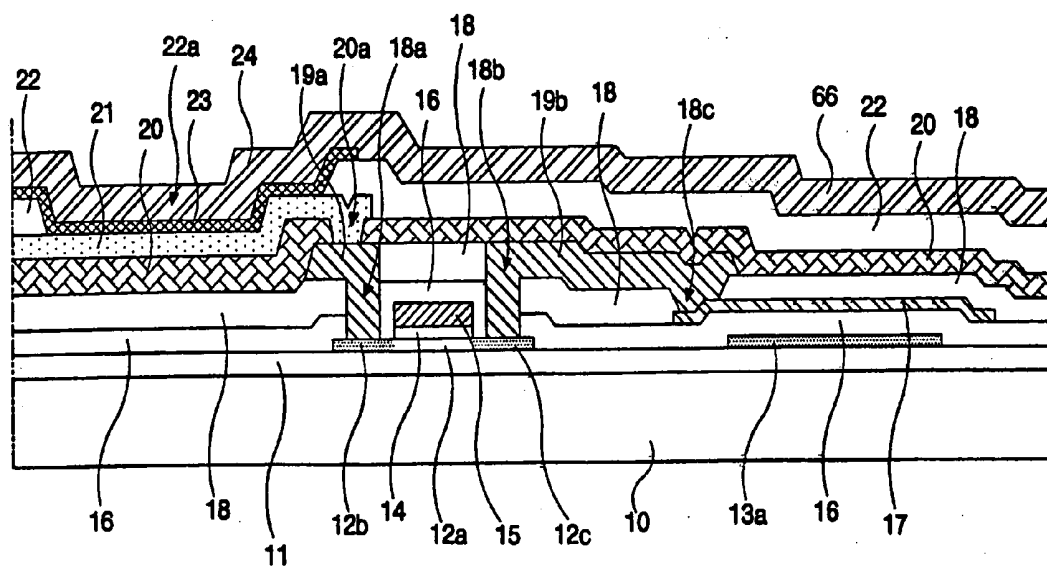


FIG. 2
(Related Art)

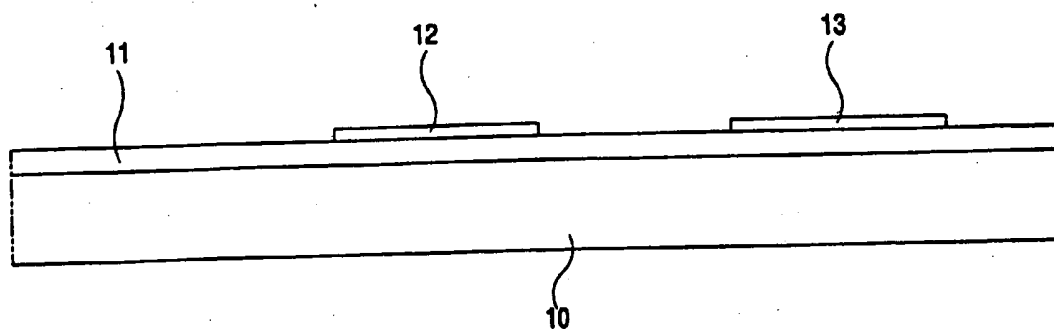


FIG. 3A
(Related Art)

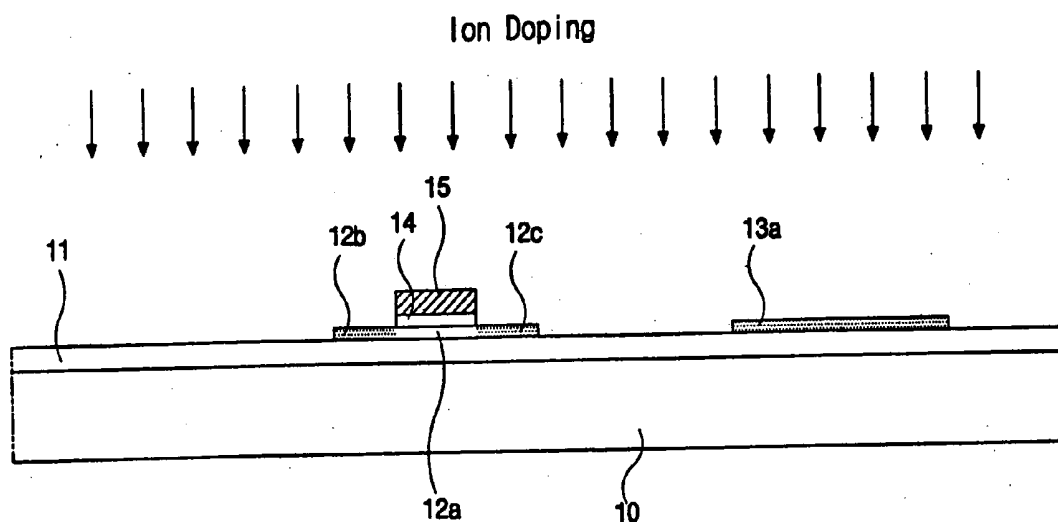


FIG. 3B
(Related Art)

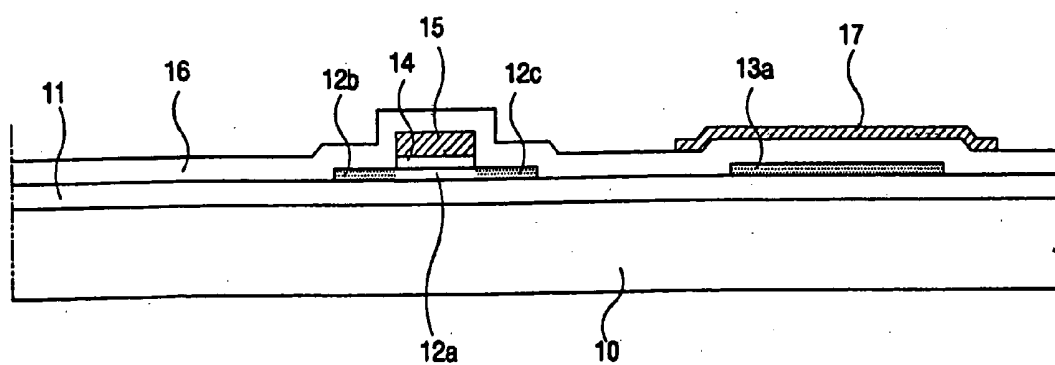


FIG. 3C
(Related Art)

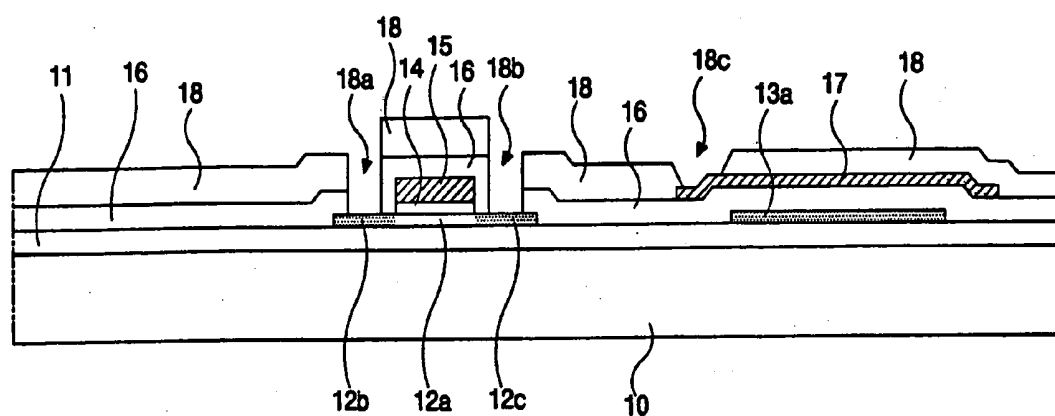


FIG. 3D
(Related Art)

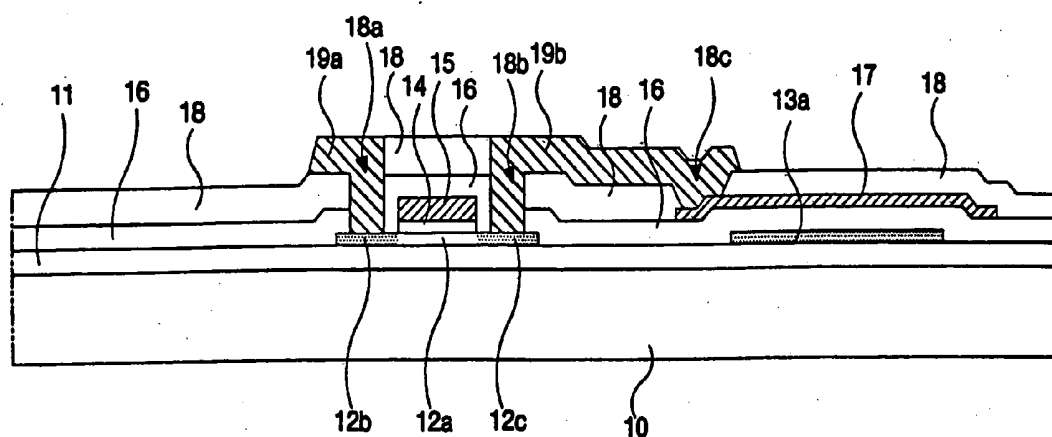


FIG. 3E
(Related Art)

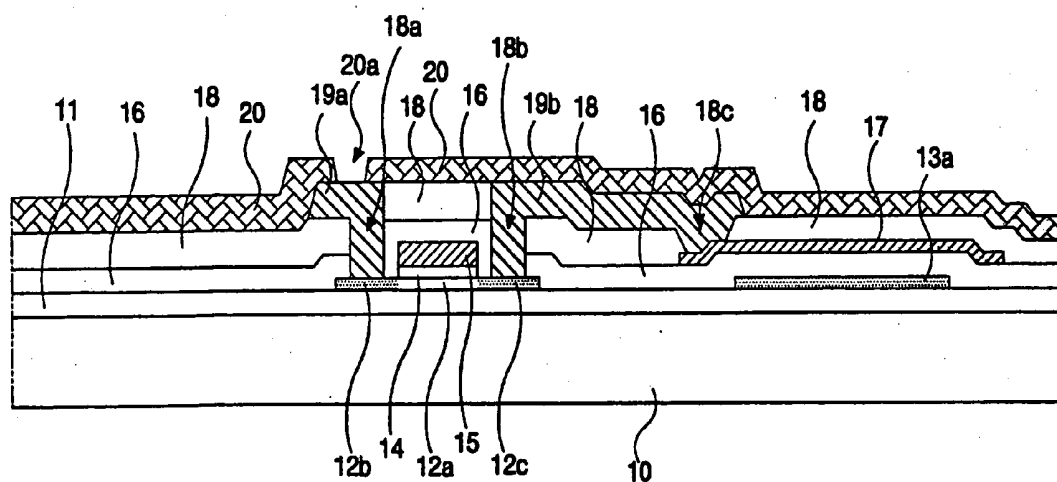


FIG. 3F
(Related Art)

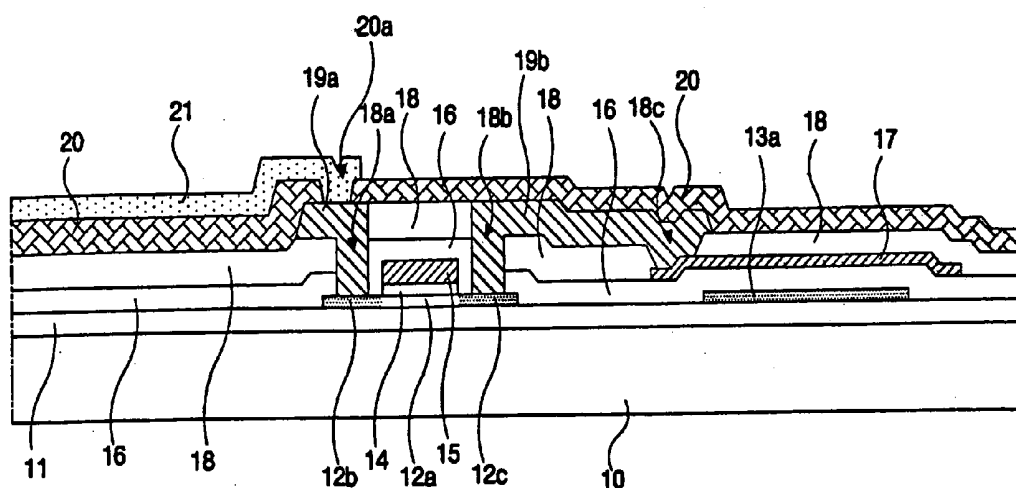


FIG. 3G
(Related Art)

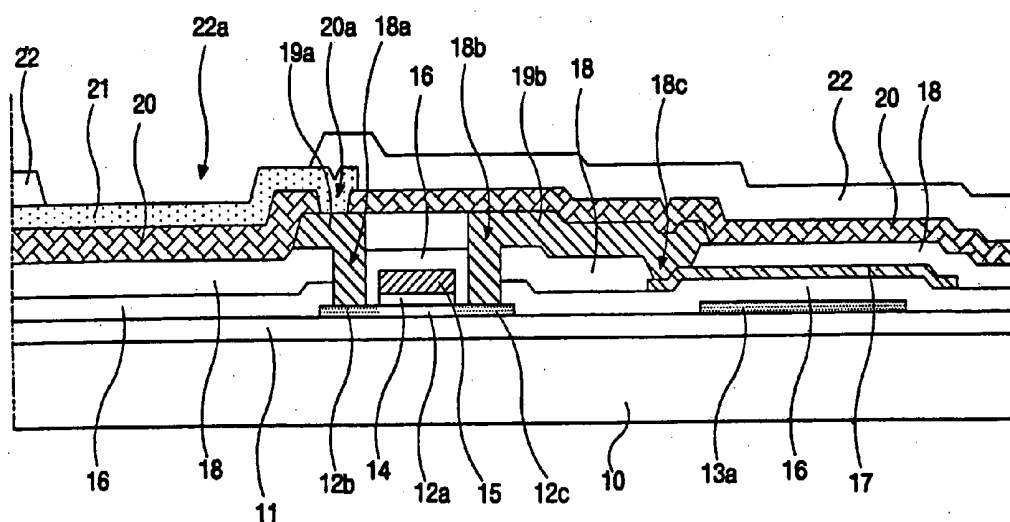


FIG. 3H
(Related Art)

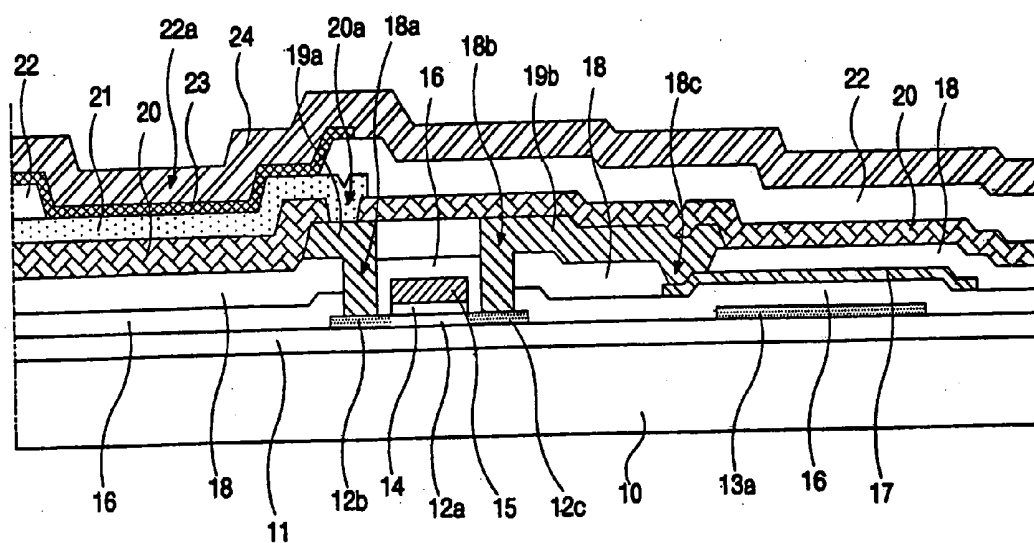


FIG. 3I
(Related Art)

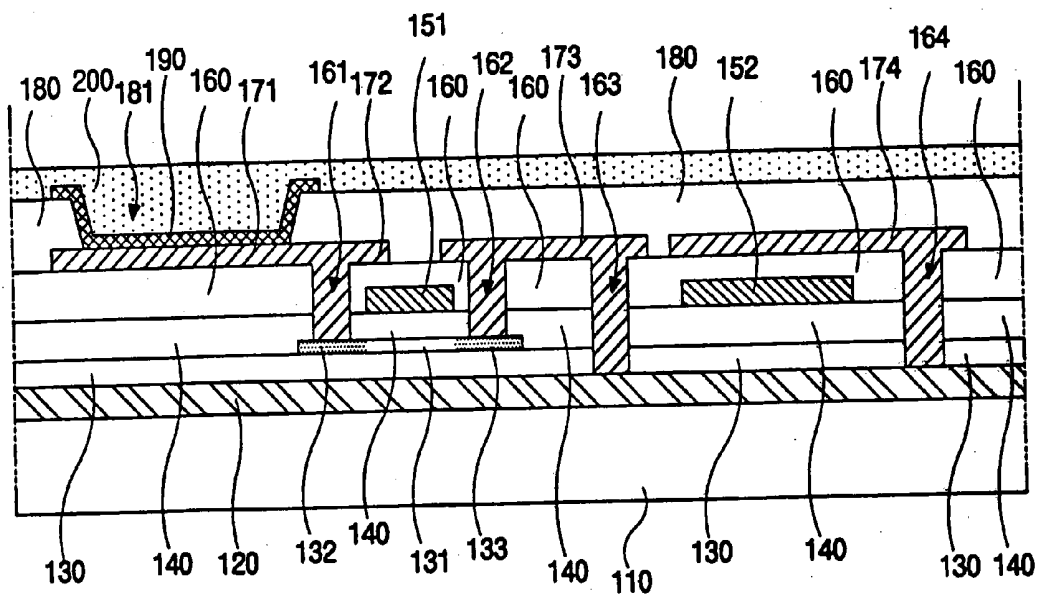


FIG. 4

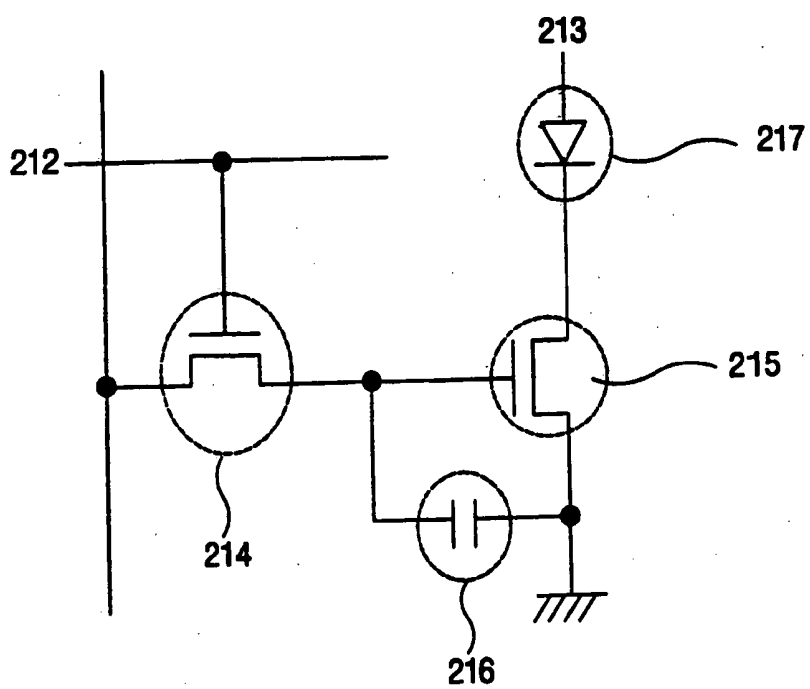


FIG. 5

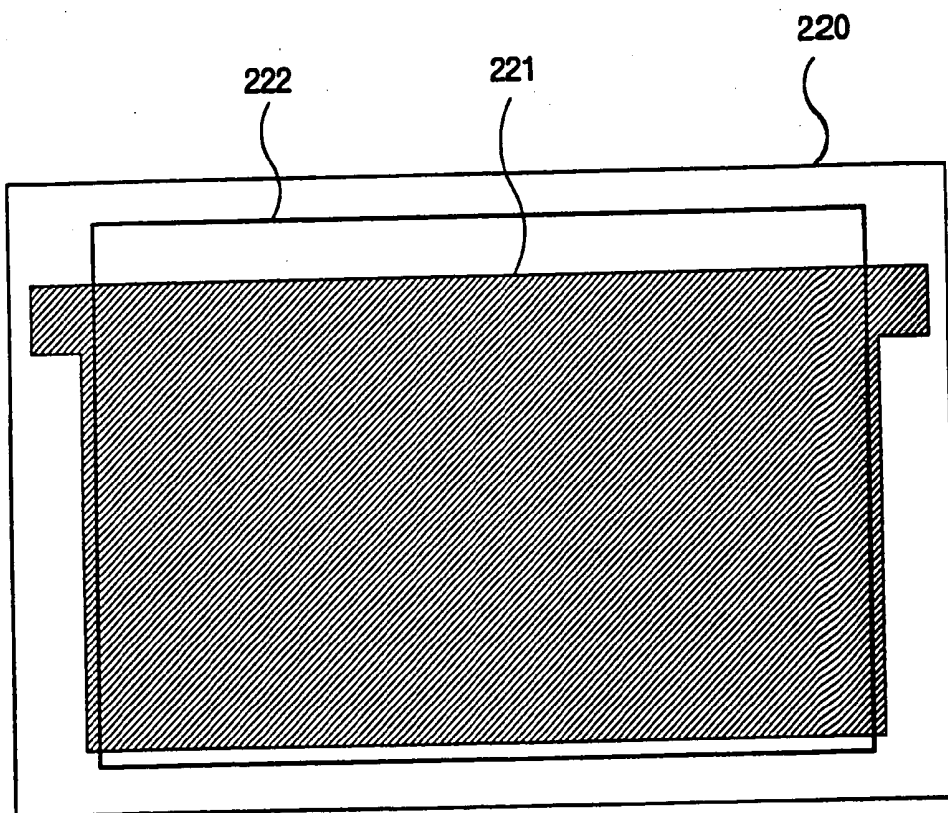


FIG. 6

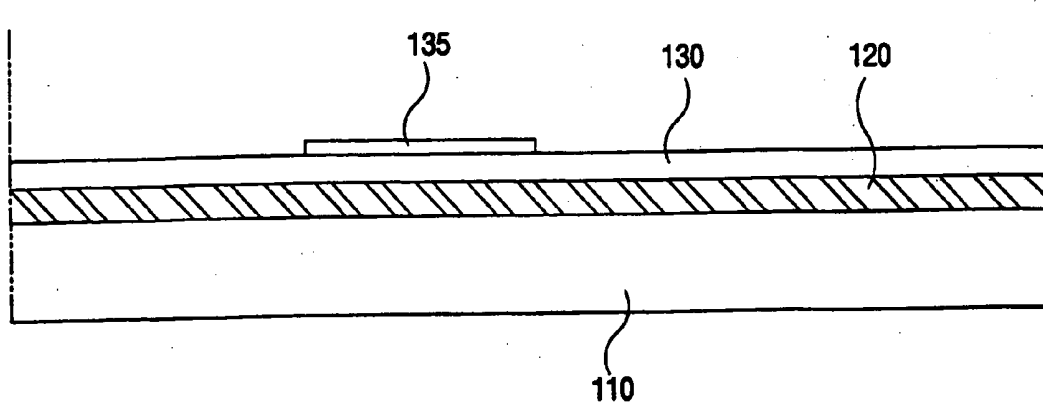


FIG. 7A

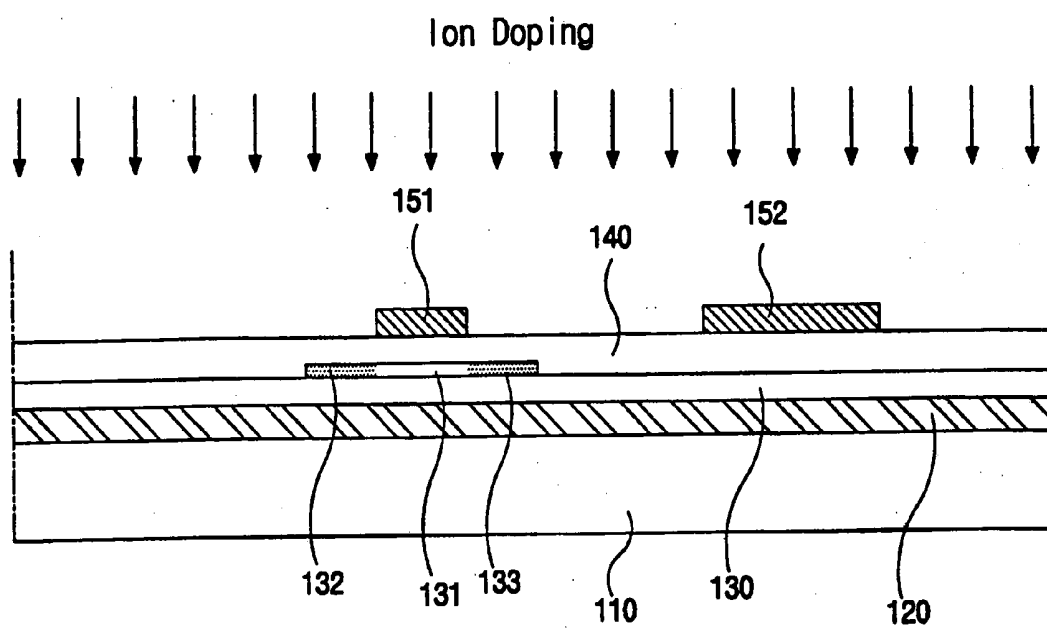


FIG. 7B

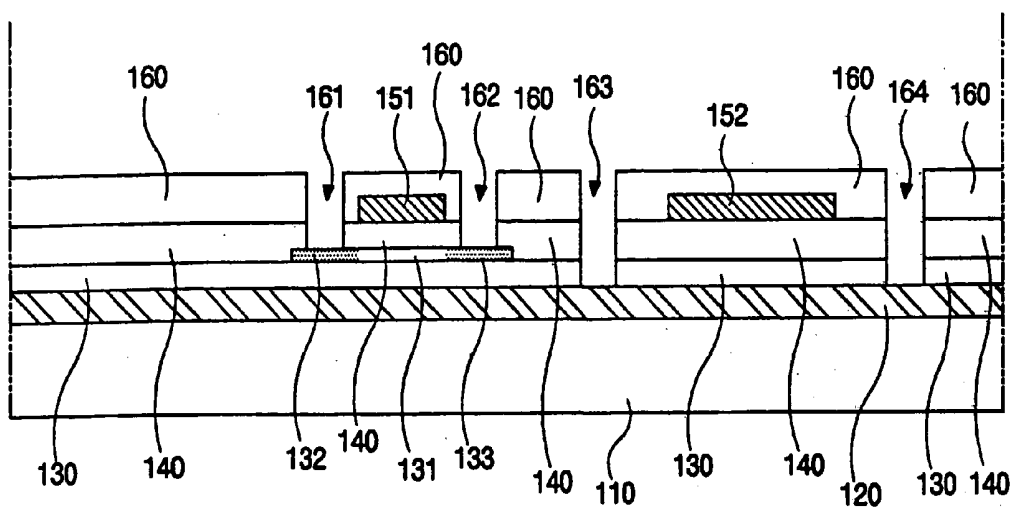


FIG. 7C

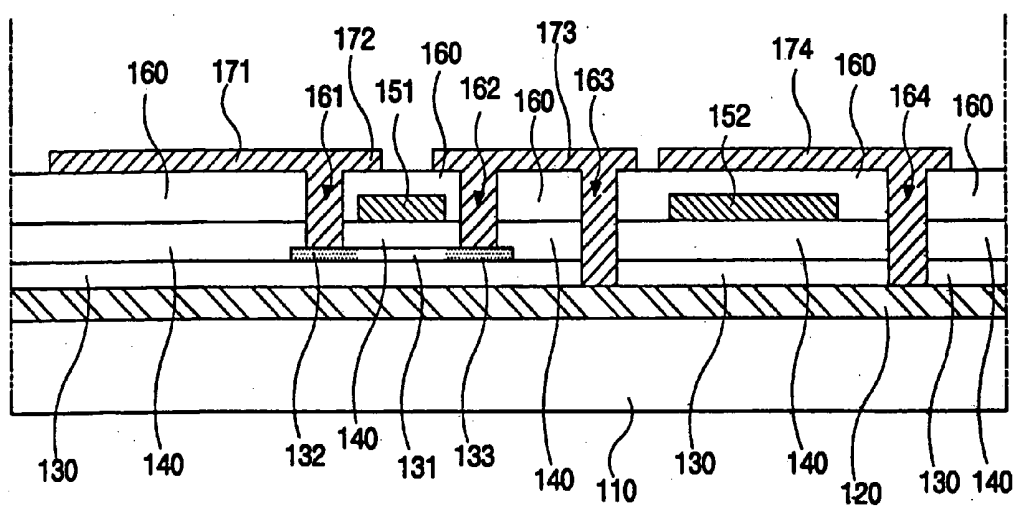


FIG. 7D

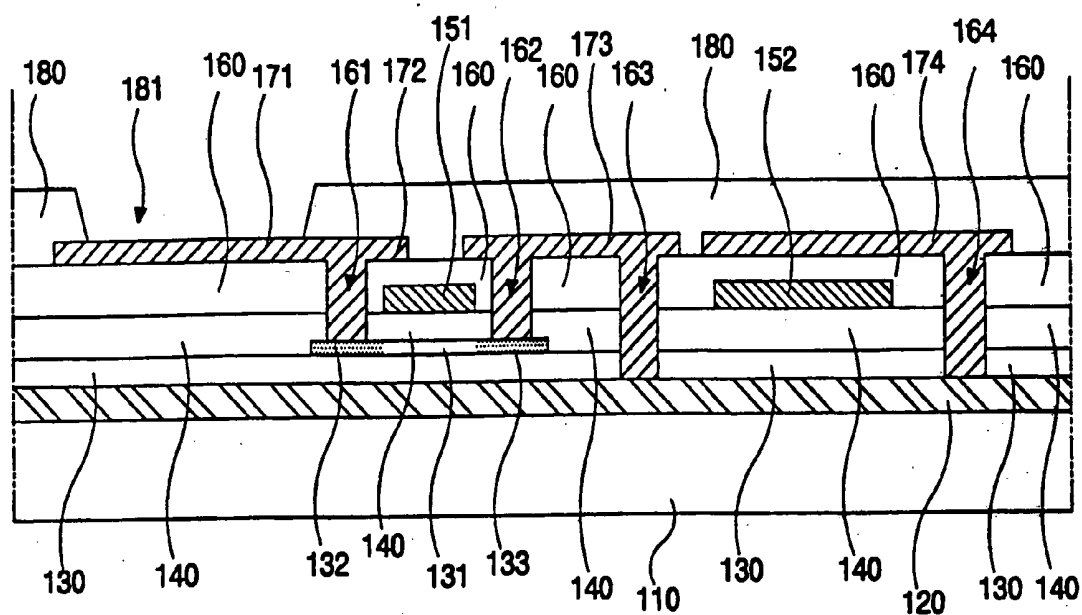


FIG. 7E

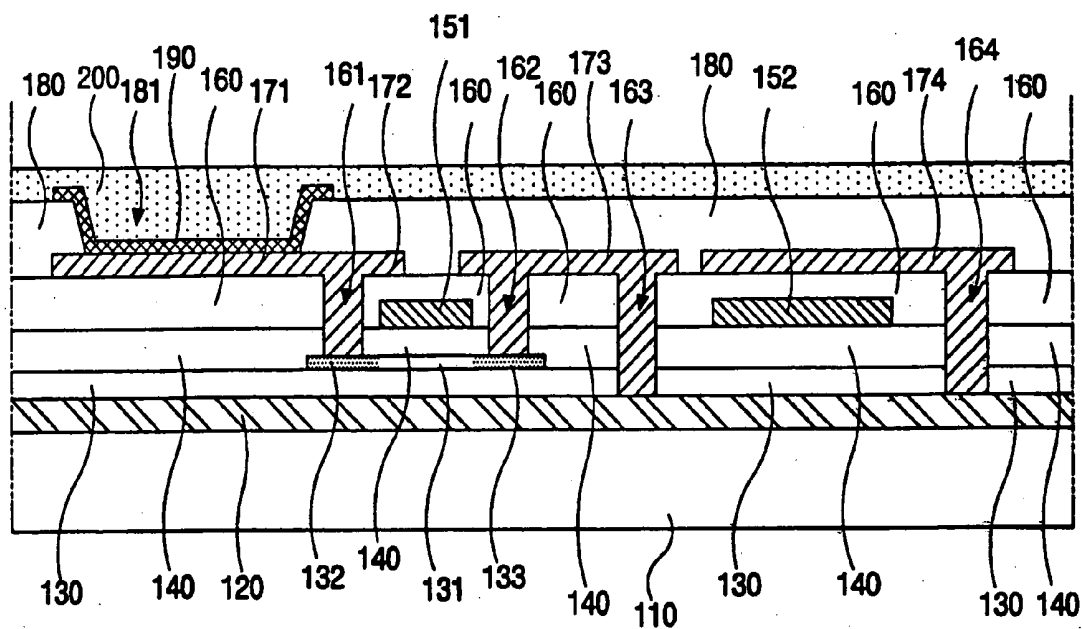


FIG. 7F

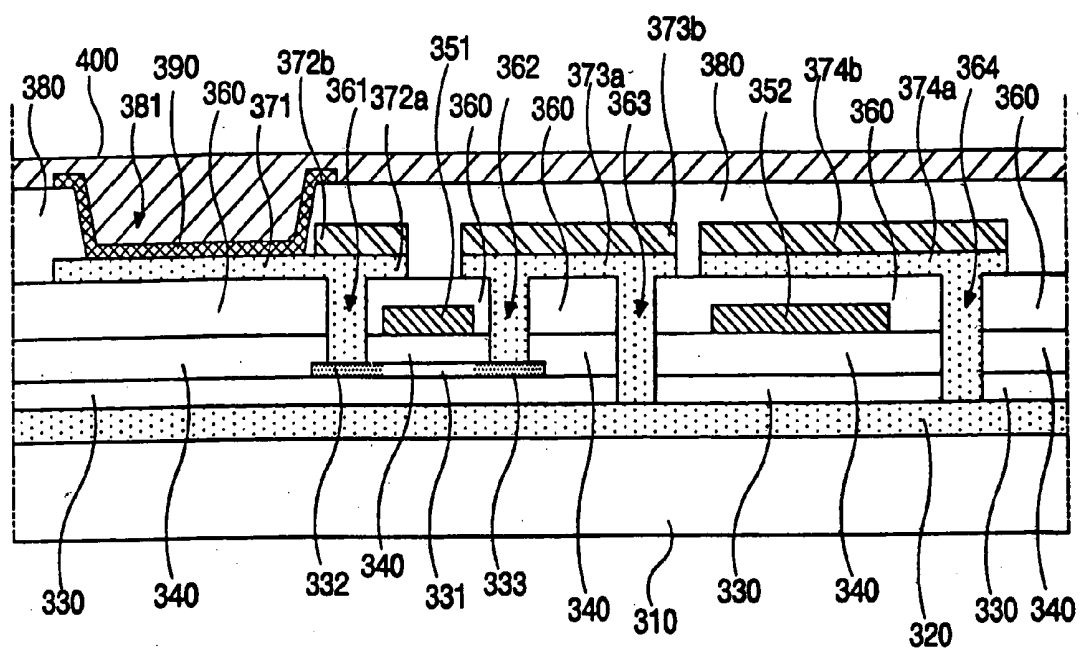


FIG. 8

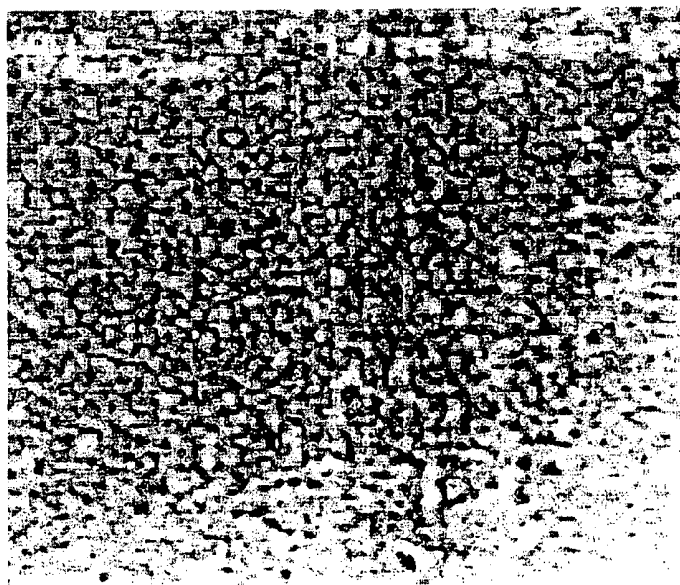


FIG. 9

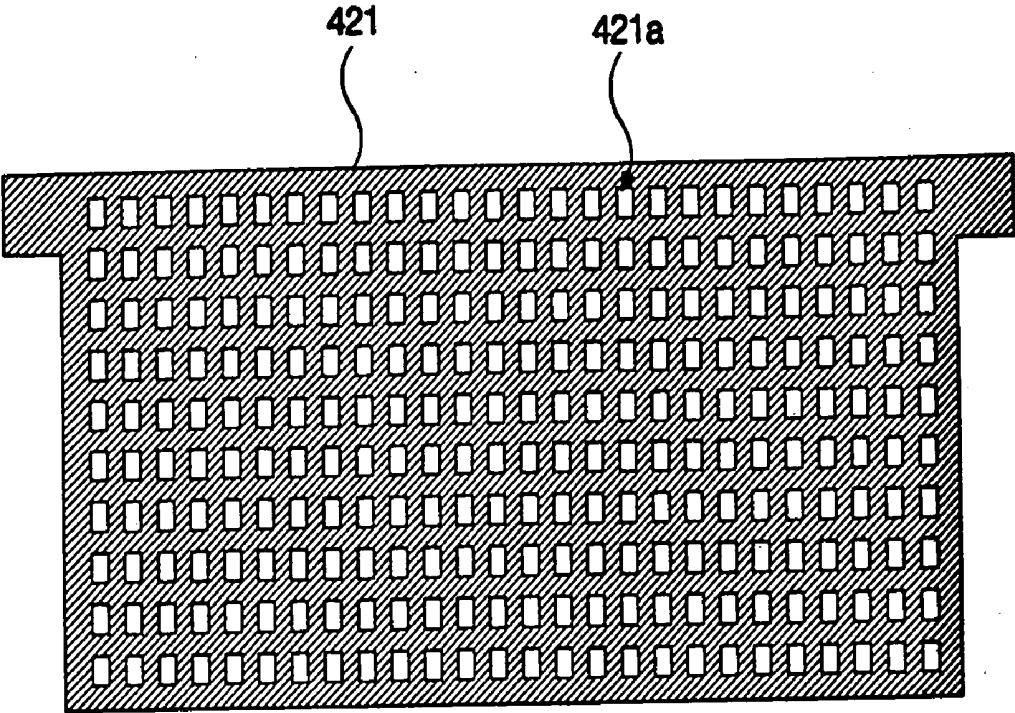


FIG. 10

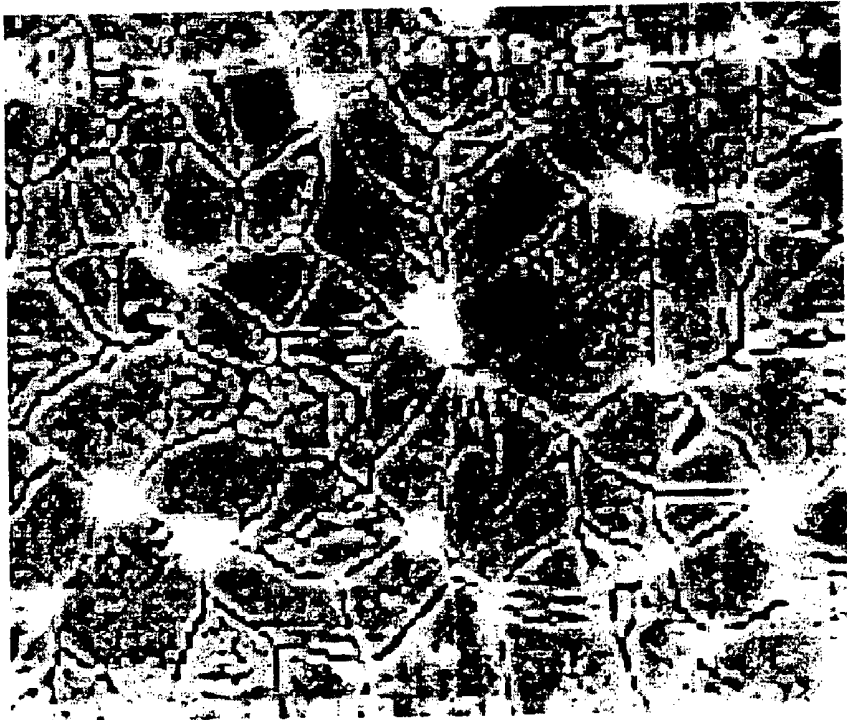


FIG. 11

ACTIVE MATRIX ORGANIC ELECTROLUMINESCENT DISPLAY DEVICE AND FABRICATING METHOD THEREOF

[0001] This application claims the benefit of Korean Patent Application No. 2001-0088538 filed on Dec. 29, 2001, which is hereby incorporated by reference in its entirety for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to organic electroluminescent display devices, and more particularly, to an active matrix electroluminescent display devices having thin film transistors.

[0004] 2. Discussion of the Related Art

[0005] As an information age has been evolved rapidly, a necessity for flat panel displays, which have advantages such as thinness, lightweight and lower power consumption, has been increased. Accordingly, various flat panel display (FPD) devices such as liquid crystal display (LCD) devices, plasma display panels (PDPs), field emission display devices and electro luminescence display (ELD) devices have been researched and have been developed.

[0006] Among many kinds of FPD devices, the electroluminescence display (ELD) device makes use of electro luminescence phenomenon in which light is generated when an electric field of certain intensity is applied to a fluorescent substance. The electroluminescence display (ELD) devices can be classified into inorganic electroluminescence display (ELD) device and organic electroluminescent display (ELD) device depending on a source that excites carriers. The organic electroluminescent display (ELD) device has drawn attention as a displaying device for natural colors because it can display every color in a range of a visible light and has a high brightness and a low voltage.

[0007] In addition, because the organic electroluminescence display (ELD) device is a self-luminescent, it has a high contrast ratio and is suitable for an ultra-thin type display device. Moreover, because it has a simple manufacturing process, the degree of environmental contamination is relatively low. Besides, the organic electroluminescence display (ELD) device has a few microseconds (μ s) response time, so that it is suitable for displaying moving images. The organic electroluminescence display (ELD) device has no limit in a viewing angle and is stable in low temperature condition. Because it is driven with a relatively low voltage between 5V and 15V, a manufacturing and design of a driving circuit is easy.

[0008] A structure of the organic electroluminescent display (ELD) device is similar to that of the inorganic electroluminescence display (ELD) device, but the light-emitting theory of the organic ELD device is different from that of the inorganic ELD device. That is, the organic electroluminescent display (ELD) device emits light by a recombination of an electron and a hole, and thus it is often referred to as an organic light emitting diode (OLED).

[0009] Recently, active matrix type of ELD, in which a plurality of pixels is arranged in a matrix form and a thin film transistor is connected thereto, has been widely applied to the flat panel display devices. The active matrix type is also

applied to the organic electroluminescent display (ELD) device and this is referred to as an active matrix organic electroluminescent display (ELD) device.

[0010] FIG. 1 is an equivalent circuit diagram showing a basic pixel structure of a conventional active matrix organic electro luminescent display (ELD) device.

[0011] In FIG. 1, a pixel of the active matrix organic electroluminescent display device has a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7. The switching thin film transistor 4 and the driving thin film transistor 5 are comprised of p-type polycrystalline silicon thin film transistor. A gate electrode of the switching thin film transistor 4 is connected to the gate line 1 and a source electrode of the switching thin film transistor 4 is connected to the data line 2. A drain electrode of the switching thin film transistor 4 is connected to a gate electrode of the driving thin film transistor 5, and a drain electrode of the driving thin film transistor 5 is connected to an anode electrode of the light emitting diode (LED) 7. A cathode electrode of the light emitting diode (LED) 7 is grounded. A source electrode of the driving thin film transistor 5 is connected to a power line 3, and a storage capacitor 6 is connected to the gate electrode and the source electrode of the driving thin film transistor 5.

[0012] In the pixel structure shown in FIG. 1, if a scanning signal is applied to the gate line 1, the switching thin film transistor 4 is turned on and an image signal from the data line 2 is stored into the storage capacitor 6 through the switching thin film transistor 4. If the image signal is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light. Luminance of the light emitting diode (LED) 7 is controlled by varying an electric current of the light emitting diode (LED) 7. The storage capacitor 6 serves to keep a gate voltage of the driving thin film transistor 5 constant while the switching thin film transistor 4 is turned off. That is, because the driving thin film transistor 5 can be driven by a stored voltage in the storage capacitor 6 even when the switch thin film transistor 4 is turned off, the electric current can keep flowing into the light emitting diode (LED) 7, and thus the light emitting diode (LED) emits light until a next image signal comes in.

[0013] FIG. 2 is a schematic cross-sectional view of a related art active matrix organic electroluminescent display device. FIG. 2 shows an organic light emitting diode, a storage capacitor and a driving thin film transistor. Moreover, a bottom emission type, in which light is emitted through an anode of a lower electrode, is adopted.

[0014] In FIG. 2, a buffer layer 11 is formed on a substrate, and then a first polycrystalline silicon layer having first to third portions 12a, 12b and 12c and a second polycrystalline silicon layer 13a are formed on the buffer layer 11. The first polycrystalline silicon layer is divided into the first portion 12a (i.e., an active region) where impurities are not doped and the second and third portions 12b and 12c (i.e., respectively, a drain region and a source region) where the impurities are doped. The second polycrystalline silicon layer 13a becomes one of the capacitor electrodes. A gate insulation layer 14 is disposed on the active region 12a, and a gate electrode 15 is disposed on the gate insulation layer 14. A first interlayer insulator 16 is formed on the gate electrode 15 and on the gate insulation layer 14 while

covering the drain and source regions **12b** and **12c** and the second polycrystalline silicon layer **13a**. A power line **17** is disposed on the first interlayer insulator **16** particularly above the second polycrystalline silicon layer **13a** (i.e., the capacitor electrode). Although not shown in **FIG. 2**, the power line **17** extends as a line in one direction. The power line **17** and the second polycrystalline silicon layer **13a** with the first interlayer insulator **16** therebetween form a storage capacitor. A second interlayer insulator **18** is formed on the first interlayer insulator **16**, covering the power line **17**.

[0015] Meanwhile, first and second contact holes **18a** and **18b**, which penetrate both the first and second interlayer insulators **16** and **18**, expose the drain region **12b** and source region **12c**, respectively. Additionally, a third contact hole **18c**, which penetrates the second interlayer insulator **18**, is formed and exposes a portion of the power line **17**. A drain electrode **19a** and a source electrode **19b** are formed on the second interlayer insulator **18**. The drain electrode **19a** contacts the drain region **12b** through the first contact hole **18a**. The source electrode **19b** contacts both the source region **12c** and the power line **17**, respectively, through the second contact hole **18b** and through the third contact hole **18c**, respectively. A first passivation layer **20** is formed on the drain and source electrodes **19a** and **19b** and on the exposed portions of the second interlayer insulator **18**. The first passivation layer **20** has a fourth contact hole **20a** that exposes a portion of the drain electrode **19a**. An anode electrode **21** that is made of a transparent conductive material is disposed on the first passivation layer **20** and contacts the drain electrode **19a** through the fourth contact hole **20a**. A second passivation layer **22** is formed on the anode electrode **21** and on the exposed portions of the first passivation layer **20**. The second passivation layer **22** has a well **22a** that exposes a portion of the anode electrode **21**. An electroluminescent layer **23** is formed on the second passivation layer **22** and into the well **22a**. A cathode electrode **24** is formed entirely over the surface including on the exposed portions of the second passivation layer **22** and on the electroluminescent layer **23**. The cathode electrode **24** is formed of an opaque metallic conductive material.

[0016] In the active matrix organic electroluminescent display device illustrated in **FIG. 2**, the anode electrode **21** is formed of the transparent conductive material, while the cathode electrode **24** is formed of the opaque conductive material. Thus, the light emitted from the organic electroluminescent layer **23** is released in a bottom direction. Such device is called the bottom emission type.

[0017] **FIGS. 3A to 3I** are cross-sectional views illustrating a fabricating process of the active matrix organic electroluminescent display device of **FIG. 2**. Many of the patterns shown in **FIGS. 3A to 3G** are formed through a photolithography process of photoresist (PR) coating, aligning, exposing and developing steps using a mask.

[0018] In **FIG. 3A**, after a buffer layer **11** is formed on an entire surface of a substrate **10**, first and second semiconductor layers **12** and **13** of polycrystalline silicon are formed on the buffer layer **11** through a first mask process. The first and second polycrystalline semiconductor layers **12** and **13** have island shapes.

[0019] In **FIG. 3B**, an insulator of silicon nitride or silicon oxide and a conductive material of metal are sequentially deposited on the first polycrystalline silicon layer **12** and

then patterned using a second mask, thereby sequentially forming a gate insulation layer **12** and a gate electrode **15** on the first polycrystalline semiconductor layer **12**. Thereafter, impurities such as p-type ions are doped on the exposed portions of the first and second polycrystalline semiconductor layers **12** and **13**. During doping, the gate electrode **15** acts as a mask so that the first polycrystalline semiconductor layer **12** is divided into an active region **12a** where the impurities are not doped and drain and source regions **12b** and **12c** where the impurities are doped. Further, the second polycrystalline semiconductor layer **13** on which the impurities are fully doped becomes a capacitor electrode **13a**. The drain and source regions **12b** and **12c** are located on both sides of the active region **12a**.

[0020] Referring to **FIG. 3C**, a first interlayer insulator **16** is formed on the entire surface of the buffer layer **11** so as to cover the gate electrode **15**, the drain and source regions **12b** and **12c**, and the capacitor electrode **13a**. After forming the first interlayer insulator **16** over the entire surface of the substrate **10**, a power line **17** of metal is formed through a third mask process on the first interlayer insulator **16** particularly to overlap the capacitor electrode **13a**. Since the power line **17** is formed right above the capacitor electrode **13a**, it forms a storage capacitor with the capacitor electrode **13a** and the interposed first interlayer insulator **16**.

[0021] In **FIG. 3D**, a second interlayer insulator **18** is formed on the first interlayer insulator **16** and on the power line **17**. Thereafter, first to third contact holes **18a**, **18b** and **18c** are formed using a fourth mask process. The first contact hole **18a** exposes the drain region **12b**, the second contact hole **18b** exposes the source region **12c**, and the third contact hole **18c** exposes the power line **17**.

[0022] In **FIG. 3E**, a metal layer is formed on the second passivation layer **18** and then patterned through a fifth mask process, thereby forming a drain electrode **19a** and a source electrode **19b**. The drain electrode **19a** contacts the drain region **12b** through the first contact hole **18a**, while the source electrode **19b** contacts the source region **12c** through the second contact hole **18b**. Furthermore, the source electrode **19b** contacts the power line **17** through the third contact hole **18c**.

[0023] Through the previously described process, a driving thin film transistor having the semiconductor layer **12**, the gate electrode **15**, the drain and source electrodes **19a** and **19b** is completed. Moreover, a region corresponding to the power line **17** and the capacitor electrode **13a** forms the storage capacitor. Although not shown in **FIG. 3E**, but shown in **FIG. 1**, the storage electrode **13** is connected to the gate electrode **15** of the driving thin film transistor, and the power line **17** is parallel to the signal line.

[0024] In **FIG. 3F**, a first passivation layer **20** having a fourth contact hole **20a** resulting from a sixth mask process is formed on the second interlayer insulator while covering the drain and source electrodes **19a** and **19b**. The fourth contact hole **20a** exposes a portion of the drain electrode **19a**.

[0025] In **FIG. 3G**, a transparent conductive material is deposited on the first passivation layer **20** and then patterned using a seventh mask process, thereby forming an anode electrode **21** that contacts the drain electrode **19a** through the fourth contact hole **20a**.

[0026] In FIG. 3H, a second passivation layer 22 is formed on the anode electrode 21 and on the exposed portion of the first passivation layer 20. Thereafter, the second passivation layer 22 is patterned using an eighth mask process, thereby forming a well 22a that exposes a portion of the anode electrode 21.

[0027] Now in FIG. 3I, an organic electroluminescent layer 23 is formed on the second passivation layer to contact the anode electrode 21 through the well 22a. Thereafter, a cathode electrode 24 is formed on the organic electroluminescent layer 23 and on the exposed portion of the second passivation layer 22. The cathode electrode 24 entirely covers the substrate 10.

[0028] In the above-mentioned processes forming the organic electroluminescent display device, a plurality of thin film depositions are repeated, and moreover a plurality of photolithography processes that use masks are also repeated many times. Therefore, these repetitions increase the mask process. Since the photolithography process includes a rinsing process, a photoresist deposition process, an exposure process, a developing process, an etching process, etc., the manufacturing time and the cost of production can be reduced if only one mask process is omitted. The organic electroluminescent display device described with reference to FIGS. 3A to 3I, however, requires eight masks, resulting in a decreased production yield and increased cost of production. Moreover, the more masks the organic electroluminescent display device requires, the more defects the fabrication process creates.

[0029] Additionally, since the active matrix organic electroluminescent display device of the related art has a capacitor electrode that is an opaque material, it has a decreased luminant area and a reduced aperture ratio. In order to overcome these problems, the current density should be raised to increase the luminance of the device, thereby causing a decreased life span of the organic electroluminescent display device.

[0030] Furthermore, since the organic electro luminescent display device of the related art has the power line in a shape of line, the power line is easily deteriorated and damaged and the active matrix organic electroluminescent display device do not display images uniformly.

SUMMARY OF THE INVENTION

[0031] Accordingly, the present invention is directed to an active matrix organic electroluminescent display device that substantially obviates one or more of problems due to limitations and disadvantages of the related art.

[0032] An advantage of the present invention is to provide an active matrix organic electroluminescent display device of low fabrication cost and high production yield by reducing the number of mask processes.

[0033] Another advantage of the present invention is to provide an active matrix organic electroluminescent display device that has a high aperture ratio and a long life span.

[0034] Another advantage of the present invention is to provide an active matrix organic electroluminescent display device that prevents deterioration and damage of a power line and displays uniform images.

[0035] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. These and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0036] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an active matrix organic electroluminescent display device includes: a substrate; a ground layer on the substrate; a buffer layer on the ground layer; a polycrystalline semiconductor layer on the buffer layer, the polycrystalline semiconductor layer having an active region, a drain region and a source region, wherein the active region is disposed in the middle of the polycrystalline silicon layer and the drain and source regions are disposed in both sides of the active region; a gate insulation layer on the buffer layer to cover the polycrystalline silicon layer; a gate electrode on the gate insulation layer, the gate electrode disposed right above the active region of the polycrystalline silicon layer; a first capacitor electrode on the gate insulation layer; an interlayer insulator formed on the gate insulation layer to cover the gate electrode and the first capacitor electrode; drain and source electrodes on the interlayer insulator, the drain and source electrode contacting the drain and source regions, respectively, through first and second contact holes that penetrate the interlayer insulator and the gate insulation layer; a cathode electrode formed on the interlayer insulator and connected to the drain electrode; a second capacitor electrode on the interlayer insulator; a passivation layer formed on the interlayer insulator to cover the drain and source electrodes, the cathode electrode and the second capacitor electrode, the passivation layer having a bank that exposes the cathode electrode; an organic electroluminescent layer on the passivation layer and into the bank, the organic electroluminescent layer contacting the cathode electrode through the bank; and an anode electrode on the exposed portion of the passivation layer and on the organic electroluminescent layer.

[0037] In another aspect of the present invention, a fabricating method of an active matrix organic electroluminescent display device includes: forming a ground layer on a substrate; forming a buffer layer on the ground layer; forming a polycrystalline semiconductor layer on the buffer layer; forming a gate insulation layer on the buffer layer to cover the polycrystalline silicon layer; forming a gate electrode and a first capacitor electrode on the gate insulation layer, the gate electrode disposed right above the polycrystalline silicon layer; doping ions into the polycrystalline semiconductor layer using the gate electrode as a mask so that the polycrystalline semiconductor layer has an active region, a drain region and a source region, wherein the active region is disposed in the middle of the polycrystalline silicon layer right under the gate electrode and the drain and source regions are disposed in both sides of the active region; forming an interlayer insulator on the gate insulation layer to cover the gate electrode and the first capacitor electrode; forming first, second, third and fourth contact holes, wherein the first and second contact holes expose the drain and source regions, respectively, by penetrating both the interlayer insulator and the gate insulation layer, and the third and fourth contact holes expose portions of the ground layer by penetrating the interlayer insulator, the gate insulation layer

and the buffer layer; forming drain and source electrodes on the interlayer insulator, the drain and source electrode contacting the drain and source regions, respectively, through the first contact hole and through the second contact hole; forming a cathode electrode on the interlayer insulator, the cathode electrode connected to the drain electrode; forming a second capacitor electrode on the interlayer insulator; forming a passivation layer on the interlayer insulator to cover the drain and source electrodes, the cathode electrode and the second capacitor electrode, the passivation layer having a bank that exposes the cathode electrode; forming an organic electroluminescent layer on the passivation layer and into the bank, the organic electroluminescent layer contacting the cathode electrode through the bank; and forming an anode electrode on the exposed portion of the passivation layer and on the organic electroluminescent layer.

[0038] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0040] In the drawings:

[0041] FIG. 1 is an equivalent circuit diagram showing a basic pixel structure of a related art active matrix organic electroluminescent display (ELD) device;

[0042] FIG. 2 is a schematic cross-sectional view of a related art active matrix organic electroluminescent display device;

[0043] FIGS. 3A to 3I are cross-sectional views illustrating a fabricating process of an active matrix organic electroluminescent display device of FIG. 2.

[0044] FIG. 4 is a schematic cross-sectional view of an active matrix organic electroluminescent display device according to an exemplary embodiment of the present invention;

[0045] FIG. 5 is an equivalent circuit diagram showing a basic pixel structure of an active matrix organic electroluminescent display (ELD) device according to the present invention;

[0046] FIG. 6 is a plan view schematically illustrating a power line and a ground layer according to an exemplary embodiment of the present invention;

[0047] FIGS. 7A to 7F are cross-sectional views showing a fabricating process of an active matrix organic electroluminescent display device of FIG. 4;

[0048] FIG. 8 is a schematic cross-sectional view of an active matrix organic electroluminescent display device according to another exemplary embodiment of the present invention;

[0049] FIG. 9 is a photo showing a polycrystalline silicon layer that is formed above the ground layer shown in FIG. 6;

[0050] FIG. 10 is a plan view schematically illustrating a ground layer according to another exemplary embodiment of the present invention; and

[0051] FIG. 11 is a photo showing a polycrystalline silicon layer that is formed above the ground layer shown in FIG. 10.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0052] Reference will now be made in detail to an embodiment of the present invention, example of which is illustrated in the accompanying drawings. Wherever possible, similar reference numbers will be used throughout the drawings to refer to the similar or like parts.

[0053] FIG. 4 is a schematic cross-sectional view of an active matrix organic electroluminescent display (ELD) device according to an exemplary embodiment of the present invention. Since the active matrix organic ELD device uses a p-Si thin film transistor (TFT), a top gate type is adopted.

[0054] In FIG. 4, a ground layer 120 is formed on entire surface of a substrate 110. The ground layer 120 is a conductive material, such as metal. A buffer layer 130 of silicon nitride or silicon oxide is formed on the ground layer 120. A semiconductor layer 131 (132 and 133) that has an island-shape is formed of polycrystalline silicon on the buffer layer 130. The polycrystalline semiconductor layer is divided into an active region 131 to which dopant is not applied and drain and source regions 132 and 133 to which the dopant is applied and doped. Here, the buffer layer 130 prevents that the impurities infiltrating from the substrate 110 or the ground layer 120 into the polycrystalline semiconductor layer 131 (132 and 133). A gate insulation layer 140 is formed on the buffer layer 130, covering the active, drain and source regions 131, 132 and 133. A gate electrode 151 is formed on the gate insulation layer 140 above the active region 131 of the polycrystalline semiconductor layer. The gate electrode 151 may be formed right above the active region 131. A first capacitor electrode 152 that is made of the same material as the gate electrode 151 is formed on the gate insulation layer 140.

[0055] Still referring to FIG. 4, an interlayer insulator 160 is disposed on the gate insulation layer 140, covering the gate electrode 151 and the first capacitor electrode 152. Meanwhile, first and second contact holes 161 and 162, which penetrate both the interlayer insulator 160 and the gate insulation layer 140, expose the drain region 132 and source region 133, respectively. Additionally, third and fourth contact holes 163 and 164, which penetrate the interlayer insulator 160, gate insulation layer 140 and buffer layer 130, are formed and expose portions of the ground layer 120. A cathode electrode 171, a drain electrode 172, a source electrode 173 and a second capacitor electrode 174, which are made of an opaque conductive material, such as metal, are disposed on the interlayer insulator 160. The cathode electrode 171 is connected to the drain electrode 172 that contacts the drain region 132 through the first contact hole 161. The source electrode 173 contacts both the

drain region 133 and the ground layer 120, respectively, through the second contact hole 162 and through the third contact hole 163. The second capacitor electrode 174 contacts the ground line 120 through the fourth contact hole 164. The first and second capacitor electrodes 152 and 174 form a storage capacitor with the interposed interlayer insulator 160. Although not shown in FIG. 4, the first capacitor electrode 152 is connected to the gate electrode 151 when viewed in a superficial observation. A passivation layer 180 is formed on the interlayer insulator 160 to cover the cathode electrode 171, the drain electrode 172, the source electrode 173 and the second capacitor electrode 174. The passivation 180 has a well 181 that exposes the cathode electrode 171. An electroluminescent layer 190 is formed on the passivation layer 180 and into the well 181 so that the electroluminescent layer 190 contacts the cathode electrode 171 through the well 181. An anode electrode 200 is formed on the electroluminescent layer 190 and on the passivation layer 180. The anode electrode 200 is a transparent conductive material, such as indium tin oxide or indium zinc oxide. The anode electrode 200 is disposed entirely over the substrate 110 so that the anode electrode 200 acts as a power line.

[0056] FIG. 5 is an equivalent circuit diagram showing a basic pixel structure of an active matrix organic electroluminescent display (ELD) device according to the present invention. As shown in FIG. 5, a gate line 212 is arranged in a first direction, and a data line 211 is arranged in a second direction substantially perpendicular to the first direction, thereby defining a pixel region. Near a crossing of the data and gate lines 211 and 212, a switching thin film transistor (TFT) 214 is disposed and connected to the data and gate lines 211 and 212. The gate electrode of the switching TFT 214 is connected to the gate line 212, and the source electrode of the switching TFT 214 is connected to the data line 211. Furthermore, the switching TFT 214 is connected to both a driving thin film transistor (TFT) 215 and a storage capacitor 216. Namely, the drain electrode of the switching TFT 214 is connected to both the gate electrode of the driving TFT 215 and the capacitor electrode of the storage capacitor 216. The drain electrode of the driving TFT 215 is connected to a cathode electrode of an electroluminescent diode 217. The source electrode of the driving TFT 215 is grounded. The anode electrode of the electroluminescent diode 217 is connected to a power line 213. In order to uniformly maintain a gate voltage of the driving TFT 215, the storage capacitor 216 is connected to both the gate and source electrodes of the driving TFT 215.

[0057] In the active matrix organic electroluminescent display device illustrated in FIG. 5, it is advisable that the driving TFT 216 is an n-type thin film transistor. However, the switching TFT 215 can be either an n-type thin film transistor or a p-type thin film transistor.

[0058] As described with reference to FIG. 4, the ground layer and the power-line layer are disposed all over the substrate. FIG. 6 is a plan view schematically illustrating the ground layer 212 and the power-line layer 222 according to an exemplary embodiment of the present invention. In FIG. 6, the thin film transistors and the storage capacitors are omitted for simple illustration.

[0059] As illustrated in FIG. 6, the ground line 221 and the power-line layer 222 are formed over the substrate 220.

The ground layer 221 is disposed all over the substrate 220, but some portions of the substrate are exposed. Additionally, the power-line layer 222 is also disposed all over the substrate 220 so that some portions of the substrate 220 are exposed. The overlapped area of the ground line 221 and power-line layer 222 is a display region where the images appear, and thus a plurality of thin film transistors and a plurality of electroluminescent diodes are disposed in that display region. In the present invention, the power-line layer 222 acts as the anode electrode of the electroluminescent diode, as described before.

[0060] According to the present invention, since the ground layer and the power-line layer are formed all over the substrate, the resistance of the power line is reduced and the thermal damage that may be caused in the power line during driving the device is prevented. Therefore, the image quality increases and the uniformity in the display can be obtained.

[0061] In the first embodiment illustrated in FIG. 4, the cathode electrode is formed of the opaque conductive material, and the anode electrode is formed of the transparent conductive material. Thus, the organic electroluminescent display device can be a top emission type in which the light is released in an upper direction. A high aperture ratio can be obtained. As a result, the luminance of the display device can increase although the current density is not large. It is distinguishable in the present invention that the life span of the organic electroluminescent display device becomes lengthened.

[0062] FIGS. 7A to 7F are cross-sectional views illustrating a fabricating process of the active matrix organic electroluminescent display device of FIG. 4.

[0063] In FIG. 7A, a conductive material, such as metal, is deposited on a substrate 110 and then patterned using a first mask process to form a ground line 120. When viewed in a superficial observation, the ground line 120 has the shape shown in FIG. 6 so that it is widely disposed over the substrate 110 and covers the display region where the images appear. Thereafter, a buffer layer 130 is formed on the ground line 120. The buffer layer 130 is one of silicon oxide and silicon nitride. Next, a polycrystalline silicon layer is formed on an entire surface of the buffer layer 130 and then patterned using a second mask process to form a semiconductor layer 135. There are many ways to form the polycrystalline silicon. One is forming an amorphous silicon layer on the buffer layer and then heat-treating the amorphous silicon to form the polycrystalline silicon. Another is that a laser irradiation is used to convert the amorphous silicon into the polycrystalline silicon. In the present invention, the substrate 110 can be a glass or other transparent substances.

[0064] In FIG. 7B, a gate insulation layer 140 of silicon nitride or silicon oxide is formed on the buffer layer 130 to cover the semiconductor layer 135, and then a metallic material is deposited on the gate insulation layer 140. The deposited metallic material is patterned using a third mask process to form a gate electrode 151 and a first capacitor electrode 152. The gate electrode 151 is disposed above the semiconductor layer 135. Using the gate electrode 151 as a mask, the dopant (e.g., n-type ions) is applied to and doped on portions of the semiconductor layer 135. Thus, the semiconductor layer 135 is divided into an active region 131 in the middle and drain and source regions 132 and 133 on

both sides of the active region 131. Because the gate electrode 151 acts as a mask during the doping process, the dopant does not exist in the active region 131, but only exists in the drain and source regions 132 and 133. Although not shown in FIG. 7B, the first capacitor electrode 152 is electrically connected to the gate electrode 151.

[0065] In FIG. 7C, an interlayer insulator 160 is formed on the gate insulation layer 140 so as to cover the gate electrode 151 and the first capacitor electrode 152. Thereafter, a fourth mask process is performed to form first to fourth contact holes 161, 162, 163 and 164. The first and second contact holes 161 and 162 penetrate both the interlayer insulator and the gate insulation layer 140, and respectively expose the drain region 132 and the source region 133. Additionally, the third and fourth contact holes 163 and 164 penetrate the interlayer insulator 160, the gate insulation layer 140 and the buffer layer 130 so that they expose portions of the ground layer 120.

[0066] In FIG. 7D, a conductive material, such as metal, is deposited on the interlayer insulator 160 and then patterned using a fifth mask process so as to form a cathode electrode 171, a drain electrode 172, a source electrode 173 and a second capacitor electrode 174. The cathode electrode 171 is connected to the drain electrode 172, as shown in FIG. 7D. The drain electrode 172 contacts the drain region 132 through the first contact hole 161. The source electrode 173 contacts the source region 133 and the ground line 120 through the second contact hole 162 and through the third contact hole 163, respectively. Furthermore, the second capacitor electrode 174 contacts the ground line 120 through the fourth contact hole 164 and forms the storage capacitor with the first capacitor electrode 152 and the interposed interlayer insulator 160.

[0067] Now in FIG. 7E, a passivation layer 180 is formed on the patterned conductive layer and on the exposed portions of the interlayer insulator 160. Thus, the passivation layer 180 covers the cathode electrode 171, the drain electrode 172, the source electrode 173 and the second capacitor electrode 174. Thereafter, a portion of the passivation layer 180 is patterned through a sixth mask process, thereby resulting in a well 181 that exposes the cathode electrode 171.

[0068] In FIG. 7F, an organic electroluminescent layer 190 is formed on the passivation layer 180 and on the exposed cathode electrode 171. The organic electroluminescent layer 190 contacts the cathode electrode 171 through the well 181. Thereafter, a transparent conductive material, such as indium tin oxide or indium zinc oxide, is formed on the organic electroluminescent layer 190 and on the passivation layer 180, thereby forming an anode electrode 200. At the time of forming the organic electroluminescent layer 190, an inkjet method or a shadow mask is used so that an additional mask process is not required. Furthermore, since the shadow mask is also used to form the anode electrode 200, the additional mask process is not required either.

[0069] As described with reference to FIGS. 7A to 7F, the active matrix organic electroluminescent display device of the present invention is fabricated through the first to sixth mask processes. Thus, the fabrication time and the cost of production are dramatically reduced as compared with the related art. Furthermore, it is possible that the defects of the

layer elements is lessened because the reduction of the mask process. Accordingly, the fabrication yield increases in the present invention.

[0070] The active matrix organic electroluminescent display device shown in FIGS. 4 and 7A-7F is the top emission type. However, the principles of the present invention can be adopted in the bottom emission type device. The active matrix organic electroluminescent display device of the bottom emission type will be described in detail with reference to FIG. 8.

[0071] FIG. 8 is a schematic cross-sectional view of an active matrix organic electroluminescent display device according to another exemplary embodiment of the present invention.

[0072] As shown in FIG. 8, a ground line 320 of a transparent conductive material is entirely formed on a substrate 310. The transparent conductive material may be indium tin oxide (ITO) or indium zinc oxide (IZO) or the like, and the substrate 310 is substantially a glass, for example. A buffer layer 330 is formed on the ground line 320. A semiconductor layer having an active region 331, drain region 332 and source region 333 is formed on the buffer layer 330. The semiconductor layer is formed of polycrystalline silicon and shaped like an island. The active layer 331 is a pure silicon region to which no dopant is applied. The drain and source regions 332 and 333 disposed on both sides of the active layer 331 are impurity-doped regions where the dopant is applied and doped.

[0073] Thereafter, a gate insulation layer 340 is formed on the buffer layer 330, covering the active, drain and source regions 331, 332 and 333. A gate electrode 351 is formed on the gate insulation layer 340 particularly right the active region 331 of the polycrystalline semiconductor layer. The gate electrode 351 may be formed right above the active region 331. Further, a first capacitor electrode 352 that is made of the same material as the gate electrode 351 is formed on the gate insulation layer 340. Although not shown in FIG. 8, the gate electrode 351 and the first capacitor electrode 352 are electrically connected to each other. Next, an interlayer insulator 360 is disposed on the gate insulation layer 340, covering the gate electrode 351 and the first capacitor electrode 352.

[0074] Meanwhile, first and second contact holes 361 and 362, which penetrate both the interlayer insulator 360 and the gate insulation layer 340, are formed to expose the drain region 132 and source region 133, respectively. Additionally with the first and second contact holes 361 and 362, third and fourth contact holes 163 and 164, which penetrate the interlayer insulator 160, gate insulation layer 140 and buffer layer 130, are formed to expose portions of the ground layer 320. A cathode electrode 371, a drain electrode 372, a source electrode 373 and a second capacitor electrode 374 are disposed on the interlayer insulator 360. The cathode electrode 371 has a single-layered structure, while the drain electrode 372, the source electrode 373 and the second capacitor electrode 374 have a double-layered structure. The cathode electrode 371 is made of a transparent conductive material, such as indium tin oxide (ITO) or indium zinc oxide (IZO), for example. Further, the lower part 372a of the drain electrode 372, the lower part 373a of the source electrode 373 and the lower part 374a of the second capacitor electrode 374 are also made of the transparent conductive

material, for example, indium tin oxide (ITO) or indium zinc oxide (IZO). On the contrary, the upper part **372b** of the drain electrode **372**, the upper part **373b** of the source electrode **373** and the upper part **374b** of the second capacitor electrode **374** are made of an opaque conductive material, such as metal, for example. The cathode electrode **371** is connected to the lower part **372a** of the double-layered drain electrode **372**, which contacts the drain region **332** through the first contact hole **361**. The lower part **373a** of the source electrode **373** contacts both the drain region **333** and the ground layer **320** through the second contact hole **362** and through the third contact hole **363**, respectively. The lower part **374a** of the second capacitor electrode **374** contacts the ground line **320** through the fourth contact hole **364**. The first and second capacitor electrodes **352** and **374** form a storage capacitor with the interposed interlayer insulator **360**.

[0075] Next, a passivation layer **380** is formed on the interlayer insulator **360** to cover the cathode electrode **371**, the drain electrode **372**, the source electrode **373** and the second capacitor electrode **374**. The passivation layer **380** has a well **381** that exposes the cathode electrode **371**. An electroluminescent layer **390** is then formed on the passivation layer **380** and into the well **381** so that the electroluminescent layer **390** contacts the cathode electrode **371** through the well **381**. An anode electrode **400** is formed on the electroluminescent layer **390** and on the passivation layer **380**. Here, it is distinguishable that the anode electrode **400** is formed of an opaque conductive material, such as metal, for example. The anode electrode **400** is disposed entirely over the substrate **310** so that the anode electrode **400** acts as a power line.

[0076] In the exemplary example of the organic electroluminescent display device shown in **FIG. 8**, the ground layer **320** and the power-line anode layer **400** are formed all over the substrate **310**. Thus, the resistance of the power line is reduced, and the thermal damage that may occur in the power line during driving the device is prevented. Therefore, the image quality increases and the uniformity in the display can be obtained. Moreover, since the ground line **320** and the cathode electrode **371** are made of the transparent conductive layer and the anode electrode **400** acting as the power line is made of the opaque conductive material, the active matrix organic electro luminescent display device of **FIG. 8** becomes the bottom emission type in which the light is released in the bottom direction.

[0077] When fabricating the active matrix organic electroluminescent display device, a six-mask process can be adopted as like the first embodiment of **FIGS. 7A to 7F**. In order to use only six masks in the fabrication of the device shown in **FIG. 8**, the double layers of the transparent conductive material and the opaque conductive material are sequentially formed on the interlayer insulator **360**. Thereafter, an exposure process is conducted using a special mask that has a slit in a portion for the cathode electrode **371**. Thus, the six-mask process is available even though the drain and source electrodes **372** and **373** and the second capacitor electrode **374** have the double-layered structure.

[0078] Meanwhile, the polycrystalline semiconductor layer having the active, drain and source regions are formed by applying heat or laser beam to the deposited amorphous silicon layer. However, since the ground layer is disposed on

the entire of the substrate and then the amorphous silicon layer is formed above the ground layer in the above-mentioned structures, the amorphous silicon layer is not properly crystallized because the applied heat for crystallization is dispersed by ground layer having high thermal conductivity. This heat dispersion phenomenon induces a long crystallization time and produces inappropriate polycrystalline silicon. The polycrystalline silicon layer formed right above the ground layer is shown in **FIG. 9**. As shown in **FIG. 9**, the grains of the polycrystalline silicon are relatively small so that the thin film transistor having these small grain sizes does not have good electrical properties and characteristics. Specifically, when using the laser beam for crystallization, the crystallization becomes worse because the light energy of the laser beam more easily disperses through the ground layer.

[0079] Therefore, to overcome this problem of thermal or light energy dispersion, another embodiment of the present invention provides a ground layer that has a plurality of openings each corresponding in position to the semiconductor layer. The ground layer having the plurality of openings is illustrated in **FIG. 10**. The ground layer **421** has the plurality of openings **421a** therein in a row-and-column formation. Each opening **421a** corresponds to a thin film transistor, especially to the semiconductor layer having the active, drain and source regions. When using the ground layer **421** of **FIG. 10**, the semiconductor layer of polycrystalline silicon can have the large grains.

[0080] **FIG. 11** is a photo showing the polycrystalline silicon layer that is formed above the ground layer shown in **FIG. 10**. Due to the opening **421a** of the ground layer **421**, the amorphous silicon is not deprived of the thermal or light energy when the amorphous silicon is crystallized. Thus, the grains of polycrystalline semiconductor layer become larger as shown in **FIG. 11**. The thin film transistor having this large-sized polycrystalline silicon semiconductor layer can have the good electrical properties and characteristics.

[0081] The illustrated embodiments of the present invention have the following advantages.

[0082] First, since the ground line and the power line are entirely disposed above the substrate, the resistance of the power line is reduced and the thermal damage that may occur in the power line during driving the device is prevented. Therefore, the image quality increases and the uniformity in the display can be obtained.

[0083] Second, since the cathode electrode are formed with the drain and source electrode at the same time, the fabrication process can be reduced and the cost of production is lowered. Further, defect occurrence is reduced due to the process reduction, and the production yield can be raised.

[0084] Third, the principles of the present invention can be applied to either the top emission type organic electroluminescent display device or the bottom emission type organic electroluminescent display device. When it is utilized for the top emission type, the active matrix organic electroluminescent display device can have a high aperture ratio.

[0085] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present inven-

tion cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1-24. (canceled)

25. A method of fabricating an active matrix organic electroluminescent device, comprising:

forming a ground layer on a substrate;

forming a buffer layer on the ground layer;

forming a polycrystalline semiconductor layer on the buffer layer;

forming a gate insulation layer on the buffer layer to cover the polycrystalline silicon layer;

forming a gate electrode and a first capacitor electrode on the gate insulation layer, the gate electrode disposed above the polycrystalline silicon layer;

doping ions into the polycrystalline semiconductor layer using the gate electrode as a mask so that the polycrystalline semiconductor layer has an active region, a drain region and a source region, wherein the active region is disposed in the middle of the polycrystalline silicon layer and under the gate electrode and the drain and source regions are disposed to both sides of the active region;

forming an interlayer insulator on the gate insulation layer to cover the gate electrode and the first capacitor electrode;

forming first, second, third and fourth contact holes, wherein the first and second contact holes expose the drain and source regions, respectively, by penetrating both the interlayer insulator and the gate insulation layer, and the third and fourth contact holes expose portions of the ground layer by penetrating the interlayer insulator, the gate insulation layer and the buffer layer;

forming drain and source electrodes on the interlayer insulator, the drain and source electrode contacting the drain and source regions, through the first contact hole and through the second contact hole, respectively;

forming a cathode electrode on the interlayer insulator, the cathode electrode connected to the drain electrode;

forming a second capacitor electrode on the interlayer insulator;

forming a passivation layer on the interlayer insulator to cover the drain and source electrodes, the cathode electrode and the second capacitor electrode, the passivation layer having a well that exposes the cathode electrode;

forming an organic electroluminescent layer on the passivation layer and into the well, the organic electroluminescent layer contacting the cathode electrode through the well; and forming an anode electrode on the exposed portion of the passivation layer and on the organic electroluminescent layer.

26. The method according to claim 25, wherein the gate electrode is electrically connected to the first capacitor electrode.

27. The method according to claim 26, wherein the gate electrode and the first capacitor electrode are formed of the same material.

28. The method according to claim 25, wherein the source electrode contacts the ground line through the third contact hole that exposes the portion of the ground layer.

29. The method according to claim 25, wherein the second capacitor electrode contacts the ground line through the fourth contact hole that exposes the portion of the ground layer.

30. The method according to claim 25, wherein the anode electrode is disposed all over the substrate and acts as a power line.

31. The method according to claim 25, wherein the first and second capacitor electrodes with the interlayer insulator layer interposed therebetween form a storage capacitor.

32. The method according to claim 25, wherein the drain and source regions of the polycrystalline semiconductor layer are doped with ions, and the active region remains of pure silicon.

33. The method according to claim 25, wherein forming the ground layer includes forming a plurality of openings therein each corresponding in position to the polycrystalline semiconductor layer.

34. The method according to claim 25, wherein the ground layer is formed of an opaque conductive material.

35. The method according to claim 34, wherein the opaque conductive material is metal.

36. The method according to claim 34, wherein forming the drain and source electrodes, forming the cathode electrode and forming the second capacitor electrode are performed during the same mask process using the opaque conductive material.

37. The method according to claim 36, wherein the opaque conductive material is metal.

38. The method according to claim 34, wherein the anode electrode is formed of a transparent conductive material.

39. The method according to claim 38, wherein the transparent conductive material includes one of indium tin oxide and indium zinc oxide.

40. The method according to claim 25, wherein the ground layer is formed of a transparent conductive material.

41. The method according to claim 40, wherein the transparent conductive material is one of indium tin oxide and indium zinc oxide.

42. The method according to claim 40, wherein forming the drain and source electrodes, forming the cathode electrode and forming the second capacitor electrode are performed at the same time using a same mask and using the same material of an opaque conductive material.

43. The method according to claim 42, wherein the mask has a slit in a position corresponding to the cathode electrode.

44. The method according to claim 43, wherein the cathode electrode has a single-layered structure of a transparent conductive material, wherein the transparent conductive material is one of indium tin oxide and indium zinc oxide.

45. The method according to claim 43, wherein the drain and source electrodes and the second capacitor electrode have a double-layered structure of a transparent conductive material and an opaque conductive material.

46. The method according to claim 45, wherein the transparent conductive material includes one of indium tin oxide and indium zinc oxide, and the opaque conductive material includes metal.

47. The method according to claim 40, wherein the anode electrode is formed of an opaque conductive material.

48. The method according to claim 47, wherein the opaque conductive material is metal.

49. The method according to claim 25, wherein the gate electrode is formed right above the active region of the polycrystalline silicon layer.

* * * * *

专利名称(译)	有源矩阵有机电致发光显示装置及其制造方法		
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摘要(译)

与使用八个掩模的现有技术不同，本发明的有源矩阵有机电致发光显示装置通过六掩模工艺制造。在本发明中，由于接地线和电源线完全设置在基板上方，所以降低了电源线的电阻，并且防止了在驱动器件期间可能在电源线中发生的热损坏。因此，图像质量增加并且可以获得显示的均匀性。此外，由于掩模工艺的减少，减少了缺陷的发生并且可以提高产量。另外，本发明的原理可以应用于顶部发射型有机电致发光显示器件或底部发射型有机电致发光显示器件。当它用于顶部发射型时，有源矩阵有机电致发光显示装置可以具有高孔径比。

